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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/028,001	FORBES ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22 and 84-99* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-22* is/are allowed.

6)☒ Claim(s) *1-14,84 and 89-99* is/are rejected.

7)☒ Claim(s) *15,16 and 85-88* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/18/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 05/18/2005 has been entered.

2. The indicated allowability of claims 1-22 and 84-99 are withdrawn in view of the newly discovered reference(s) to Endo U.S. Patent 5,619,051, Eguchi et al. U.S. Patent 5,618,761, and Shinkawata et al. U.S. Patent Application Publication 20020008324, all of which are submitted by Applicant as being cited in a copending application. Rejections based on the newly cited reference(s) follow.

Claim Rejections

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. **Claim 1, 3, 4, 84, and 90-94** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (hereinafter the '051 patent).

Referring to **claims 1, 84, and 90**, the reference discloses a floating gate transistor, comprising:

a first source/drain region (22 or 24, Fig. 5) and a second source/drain region (24 or 22) separated by a channel region (no number) in a substrate (10);

a floating gate (16) opposing the channel region and separated therefrom by a gate oxide (14);

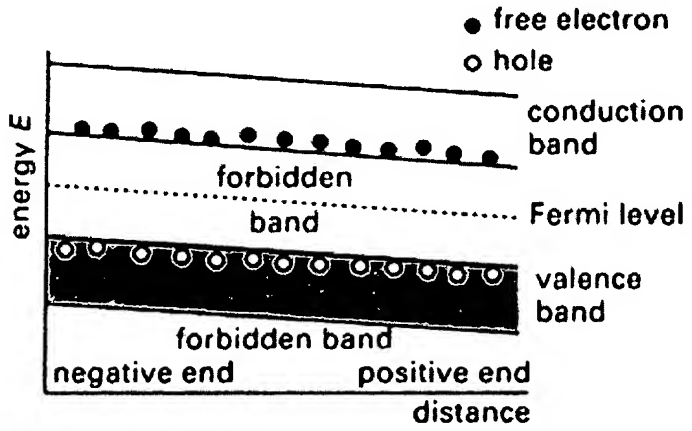
a control gate (20) opposing the floating gate; and

wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator (18A, wherein "the dielectric film 18A is formed of a solid solution of two kinds of metal oxides, and the proportions of two metal oxides vary continuously of stepwise from the bottom plane adjacent to the floating gate 16 to the top plane", column 7, lines 1-8, and where "low" is interpreted broadly, where the "tunnel barrier" property is interpreted to be inherent as the stepwise-graded dielectric layer 18A is a barrier to, for example, electrons tunneling from, for example, from the floating gate to, for example, the control gate, and where asymmetrical because the intergate insulator 18A is step-wise graded with different characteristics at the two surfaces that interface the floating gate and the control gate, as will be described in more details below) selected to provide a desired first barrier height with respect to the floating gate and a desired second barrier height with respect to the control gate, the first barrier height being different than the second barrier height to promote easier erase operations and longer retention (for the limitation a desired first barrier height with respect to the floating gate (FG), the '051 reference discloses a forbidden band width of about 3.0 eV – column 7, lines 55-60 – and the reason the forbidden band width in the instant teaching is considered functionally the same as the claimed barrier height is given below; for the limitation a desired second barrier height with respect to the control gate (CG), the '051 reference discloses a forbidden band width of about 3.4 eV – column 7, lines 55-60 – and the reason the forbidden band width in the instant teaching is considered functionally the same as the claimed barrier height is given below; for the limitation the first barrier height being different than the second barrier height, the reference teaches the first forbidden band width (3.0 eV) being different than the second forbidden

band width (3.4 eV); for the limitation to promote easier erase operations and longer retention, the reference teaches "erase time shortens to 1/5 of that in the memory cell having the dielectric film 18 of homogeneous barium strontium titanate [of a conventional device]" and "in the memory cell of FIG. 5 the information charge retention time is about twice that in the memory cell of FIG. 1 with the inter-gate dielectric film 18 of homogeneous barium strontium titanate" (paragraph bridging columns 7 and 8).

The reason the forbidden band width in the instant teaching is considered functionally the same as the claimed barrier height is given as follows:

The '051 reference teaches a stepwise-graded intergate insulator layer 18A which is as mentioned above a solid solution of two kinds of metal oxides, and the proportions of two metal oxides vary continuously of stepwise from the bottom plane adjacent to the floating gate 16 to the top plane adjacent to the CG 20. While it is true that a forbidden band width is not the same as a barrier height, it is known that in the case of non-metal, specifically in the case of metal oxide non-metal, more particular in the case of an intergate insulator as in the present situation, the barrier height (Fermi level) value lies within the forbidden band width, and this barrier height is dependent upon the characteristics of the materials (i.e., impurities or dopants, see "Semiconductor", The Online Penguin Dictionary of Physics (2000)) of the intergate insulator (see diagram below or next page)



e ENERGY BANDS *in non-metal*

energy bands. The Penguin Dictionary of Physics (2000). Retrieved 01 October 2005, from xreferplus. http://www.xreferplus.com/entry/1428694

As the material of the reference's intergate insulator ($(Ba,Sr)TiO_3$)is formed of a solid solution of two kinds of metal oxides, and the proportions of two metal oxides vary continuously of stepwise from the bottom plane adjacent to the floating gate 16 to the top plane adjacent to the CG 20, the Fermi level, or the barrier height, shall correspond to the forbidden band: when the forbidden band (value) is narrower (lower), the barrier height is lower, and when the forbidden band (value) is wider (higher), the barrier height is higher; hence according to the instant teaching, the forbidden band width is functionally the same as the claimed barrier height because the barrier height (Fermi level) is directly proportional to the forbidden band width as a result of the continuously-step-wise grading of the stepwise-graded intergate insulator layer 18A.

Although the '051 reference does not disclose a p-type channel region for the channel and an n-type for the substrate to operate the floating gate transistor in the depletion mode, such doping to operate the transistor in a depletion mode involves only routine skill in the art therefore such limitations would have been easy – hence obvious – to implement by a person of ordinary skill in the art at the time the invention was made

Referring to the limitation compositional gradients of **claims 84 and 90**, the reference's continuous-step-wise graded limitation provides the compositional gradients characteristics.

Referring to **claims 3 and 90**, the reference further discloses that that asymmetrical low tunnel barrier intergate insulator includes an asymmetrical transition metal oxide, as $SrTiO_3$ (column 7, lines 9-12) is a transition metal oxide.

Referring to **claims 4 and 91-94**, although the reference's transition metal oxide is formed of a transition metal not the same as one of the claimed transition metals, they are all transition metals, therefore their metal oxides should be functionally equivalent.

5. **Claims 9-10 and 13-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 patent) in view of Orlowski et al. U.S. Patent 6,433,382.

Referring to **claim 9**, the '051 patent discloses a non volatile memory cell substantially as claimed and as detailed above for claims 1, 84, and 90 including the asymmetrical low tunnel barrier intergate insulator 18A and a first source/drain region (22 or 24) and a second source/drain region (24 or 22) separated by a channel region (no number) in a substrate. The reference further discloses that the asymmetrical low tunnel barrier intergate insulator has a number of small compositional ranges ("the dielectric film 18A is formed of a solid solution of two kinds of metal oxides, and the proportions of two metal oxides vary continuously of stepwise from the bottom plane adjacent to the floating gate 16 to the top plane", column 7, lines 1-8) such that compositional gradients are formed to produce a first barrier height with the FG and a different barrier height with the control gate to promote easier erase operations and longer retention.

However, the reference fails to disclose a body region including the channel region and that the body region including the channel region is formed on the first source/drain region. In other words, the reference discloses a "planar" non volatile memory cell instead of a vertical non volatile memory cell as claimed.

Orlowski, in disclosing also a non volatile memory cell including a pair of source/drain regions, a channel region, a floating gate, and a control gate, teaches that vertical non volatile memory cell offers many advantages over a planar non volatile memory cell such as space saving, improved performance, reduced masking steps, and fully inverted or fully depleted channel regions (column 14, first paragraph). Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference's non volatile memory cell such that it has a vertical configuration. One would have been motivated to make

such a change because a vertical non volatile memory cell offers many advantages over a planar non volatile memory cell such as space saving, improved performance, reduced masking steps, and fully inverted or fully depleted channel regions, as taught by Orlowski.

Referring to **claim 10**, the '051 patent's material ($SrTiO_3$, column 7, lines 9-12) for the asymmetrical low tunnel barrier intergate insulator meets the limitation of the claimed Markush group of materials.

Referring to **claims 13 and 14**, the device of the '051 reference modified in view of Orlowski thus comprises a vertical floating gate (such as 30, Orlowski's Fig. 1 or Fig. 10) along side a body region (22 or 58), and a vertical control gate (32) along side the vertical floating gate.

6. **Claims 5-6 and 95-99** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 patent) as applied to claim 1 above, and further in view of Eguchi et al. U.S. Patent 5,618,761.

The '051 patent discloses a non volatile memory cell substantially as claimed and as detailed above for claim 1 including the asymmetrical low tunnel barrier intergate insulator 18A. The reference further discloses that the asymmetrical low tunnel barrier intergate insulator is formed of $SrTiO_3$ (column 7, lines 9-12) by a CVD process, meeting the limitation of claim 97 and the claimed Markush group of materials of claim 6. The reference further discloses that the asymmetrical low tunnel barrier intergate insulator ought to have a high dielectric constant (the table in column 6, lines 35-45, and claim 1). However, the reference fails to teach the limitation "Perovskite" for the asymmetrical low tunnel barrier intergate insulator.

Eguchi, in disclosing an insulator layer for a semiconductor device, teaches that a layer comprising Sr, Ti, and O formed by CVD process, has a perovskite crystal structure, which offers a high dielectric constant and excellent insulating properties (column 9, lines 37-45). Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the '051 patent's asymmetrical oxide tunnel barrier intergate insulator such that it is an asymmetrical Perovskite oxide tunnel barrier intergate insulator. One would have been motivated to make such a change because perovskite crystal structure offers a high dielectric constant and excellent insulating properties, which high dielectric constant property is desired by the '051 patent and which is taught by Eguchi.

Referring to **claims 96 and 98-99**, although the reference's transition metal oxide and the reference's modified Perovskite transition metal oxide are formed of a transition metal not the same as one of the claimed transition metals, they are all transition metals, therefore their Perovskite metal oxides should be functionally equivalent.

7. **Claims 2 and 89** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 patent) in view of Shinkawata et al. U.S. Patent Application Publication 20020008324.

The '051 patent discloses a non volatile memory cell substantially as claimed and as detailed above for claims 1 and 9 including the asymmetrical low tunnel barrier intergate insulator 18A including a number of small compositional ranges arranged in a "vary continuously of stepwise" from the bottom surface to the top surface, and wherein the number of

small compositional ranges arranged in the "vary continuously of stepwise" includes $SrTiO_3$ (column 7, lines 1-12).

However, instead of the claimed aluminum oxide (Al_2O_3), as noted, the reference discloses $SrTiO_3$.

Shinkawata, in disclosing a gate insulating film 24 for semiconductor device, teaches that the two materials are equivalent (paragraph [0063]).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the '051 patent's asymmetrical low tunnel barrier intergate insulator such that it includes aluminum oxide (Al_2O_3) instead of $SrTiO_3$. One would certainly be motivated to do that as a choice of available and art-equivalent materials.

8. **Claims 7-8 and 11-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 patent).

The '051 patent discloses a non volatile memory cell substantially as claimed and as detailed above for claims 1 and 9 including the asymmetrical low tunnel barrier intergate insulator 18A including a number of small compositional ranges arranged in a "vary continuously of stepwise" from the bottom surface to the top surface.

The reference further teaches that the floating gate includes a polysilicon floating gate having a metal silicide formed thereon (column 3, lines 56-63) in contact with the asymmetrical low tunnel barrier intergate insulator, and that the control gate includes a metal control gate having a metal oxide layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator.

Compared with the claims, the reference discloses a metal silicide instead of the claimed first metal layer for the floating gate, a metal oxide/metal instead of the claimed second metal/polysilicon for the control gate. However, the differences are deemed to be obvious to one of ordinary skill in the art at the time the invention was made ("the artisan") because at least one of the following two reasons: (1) the materials are known and available to the artisan; (2) both the present invention and the reference fails to show an advantage of one combination of materials to the other.

With respect to the limitation "wherein the metal layer includes a metal layer that has a different work function than the metal layer formed on the floating gate", the limitation appears to be inherent in the reference because: (1) the metal of the metal silicide (functionally equivalent to the claimed first metal) and the metal of the metal oxide (functionally equivalent to the claimed second metal) are different metals, resulting in different work functions; (2) the paragraph bridging columns 7 and 8, as noted above, expressly states that the forbidden band gaps, which is as detailed above for claim 1 proportional to the barrier heights, at the two surfaces of the asymmetrical low tunnel barrier intergate insulator, where the metal silicide and the metal oxide are respectively in contact with, ought to be different, leading the artisan to conclude that the work function of the metal silicide (functionally equivalent to the claimed first metal) should be different from the work function of the metal oxide (functionally equivalent to the claimed second metal).

Allowable Subject Matter

9. Claims 17-22 are allowable over the prior art of record.

Claims 15-16 and 85-88 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a non-volatile memory cell having all exclusive limitations as recited in claims 17, 15, and 85, characterized in that the second metal layer has a different work function from the first metal layer to further promote easier erase operation and longer retention (claims 17 and 85) or that the vertical p-channel depletion mode nonvolatile memory cell includes a horizontally oriented floating gate formed alongside of the body region (claim 15).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Tu-Tu Ho
October 03, 2005